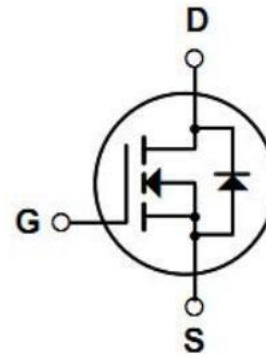


## Description

This N-Channel MOSFET uses advanced trench technology and design to provide excellent  $R_{DS(on)}$  with low gate charge. It can be used in a wide variety of applications.

## Features

- 1)  $V_{DS}=20V, I_D=6A, R_{DS(on)}<28m\ \Omega @V_{GS}=4.5V. R_{DS(on)}<35m\ \Omega @V_{GS}=2.5V.$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra  $R_{DS(on)}$ .
- 5) Excellent package for good heat dissipation.



## Absolute Maximum Ratings $T_c=25^\circ\text{C}$ , unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 10$	V
$I_D$	Continuous Drain Current-	6	A
	Continuous Drain Current- $T_c=100^\circ\text{C}$	-	
	Pulsed Drain Current <sup>1</sup>	-	
$E_{AS}$	Single Pulse Avalanche Energy	--	mJ
$P_D$	Power Dissipation	1.25	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

## Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	-	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	100	

## Package Marking and Ordering Information

Part NO.	Marking	Package
RYN20A6S	20A6S	SOT-23

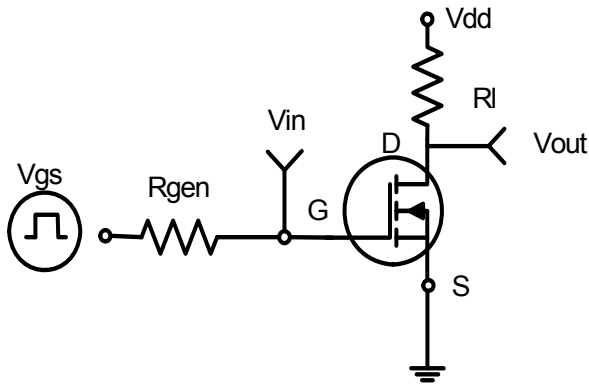
## Electrical Characteristics $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu\text{A}$	20	22		V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS}=0V, V_{DS}=20V$	-	-	-	$\mu\text{A}$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 10V, V_{DS}=0A$	-	-	$\pm 100$	nA
<b>On Characteristics<sup>3</sup></b>						
$V_{GS(th)}$	GATE-Source Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\ \mu\text{A}$	0.5	0.7	1.0	V
$R_{DS(ON)}$	Drain-Source On Resistance	$V_{GS}=4.5V, I_D=5A$	-	20	28	m $\Omega$
		$V_{GS}=2.5V, I_D=4A$	-	27	35	
$G_{FS}$	Forward Transconductance	$V_{DS}=5V, I_D=6A$	--	25	-	S
<b>Dynamic Characteristics<sup>4</sup></b>						
$C_{iss}$	Input Capacitance	$V_{DS}=10V,$ $V_{GS}=0V, f=1\text{MHz}$	-	515	---	pF
$C_{oss}$	Output Capacitance		-	90	-	
$C_{rss}$	Reverse Transfer Capacitance		-	72	--	
$R_g$	Gate Resistance	$f=1\text{MHz}$	-	-	-	$\Omega$
<b>Switching Characteristics<sup>4</sup></b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V, I_D=-A$ $V_{ds}=10V, R_{GEN}=6\ \Omega$	-	2	---	ns
$t_r$	Rise Time		-	7.5	--	ns
$t_{d(off)}$	Turn-Off Delay Time		-	20	--	ns
$t_f$	Fall Time		-	6	--	ns
$Q_g$	Total Gate Charge	$V_{GS}=10V, V_{DS}=10V,$ $I_D=6A$	-	12	10	nC
$Q_{gs}$	Gate-Source Charge		-	1	-	nC
$Q_{gd}$	Gate-Drain "Miller" Charge		-	2	-	nC
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Source-Drain Diode Forward Voltage <sup>3</sup>	$V_{GS}=0V, I_S=1A$	-	--	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=15A, di/dt=10A/\ \mu\text{S}$	-	-	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	-	-	nC

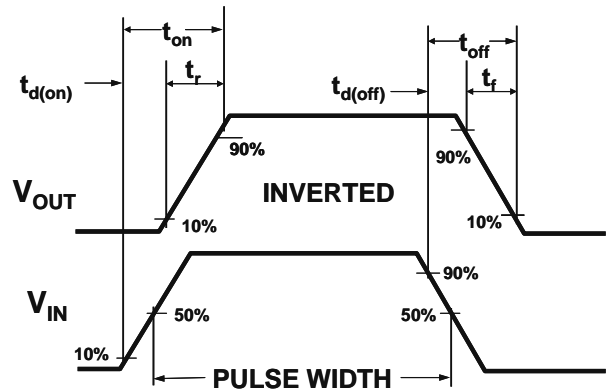
### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

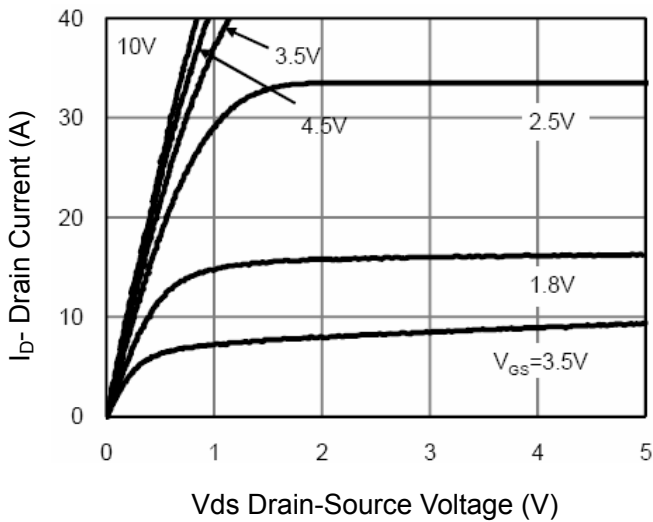
## Typical Electrical and Thermal Characteristics



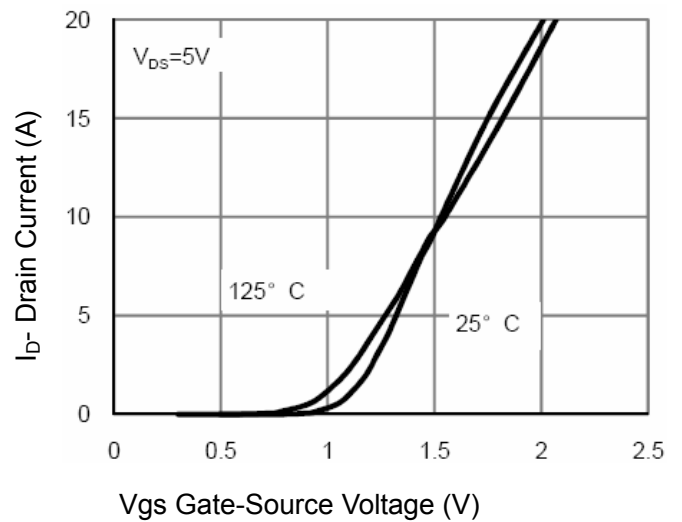
**Figure 1: Switching Test Circuit**



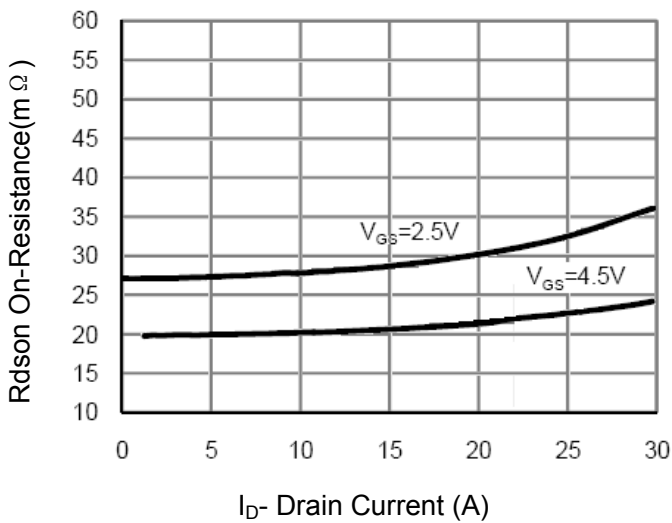
**Figure 2: Switching Waveforms**



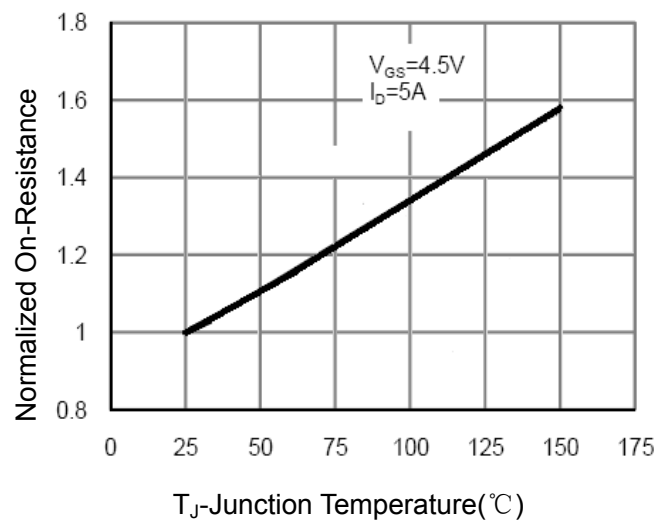
**Figure 3 Output Characteristics**



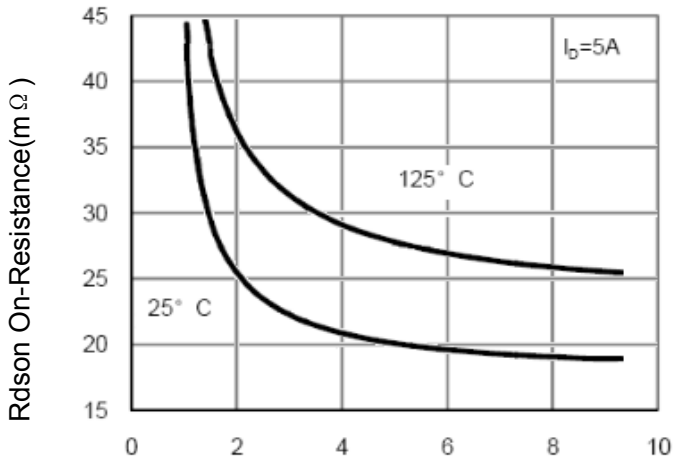
**Figure 4 Transfer Characteristics**



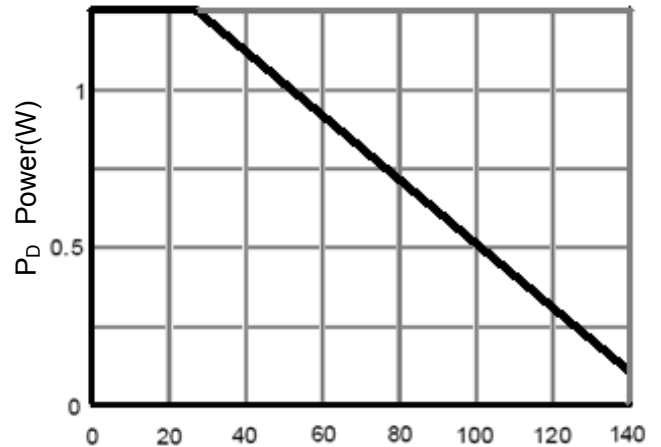
**Figure 5 Drain-Source On-Resistance**



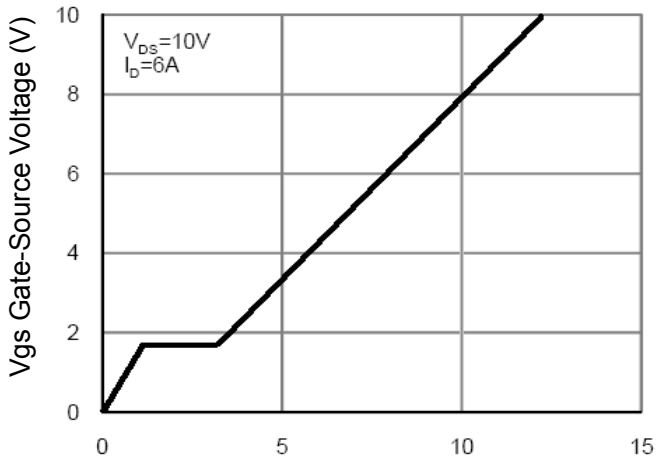
**Figure 6 Drain-Source On-Resistance**



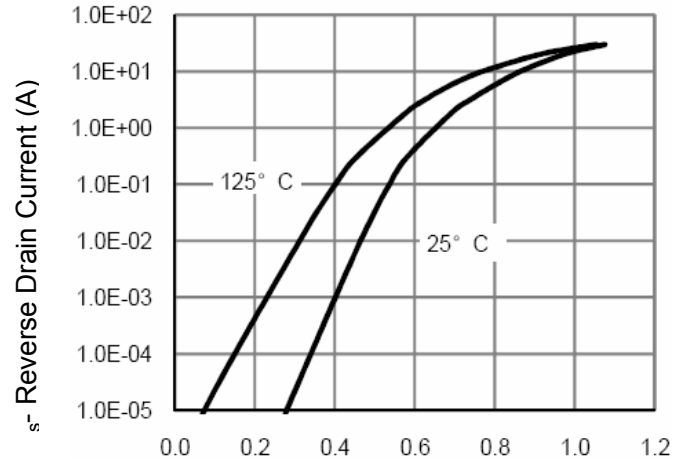
Vgs Gate-Source Voltage (V)  
**Figure 7 Rdson vs Vgs**



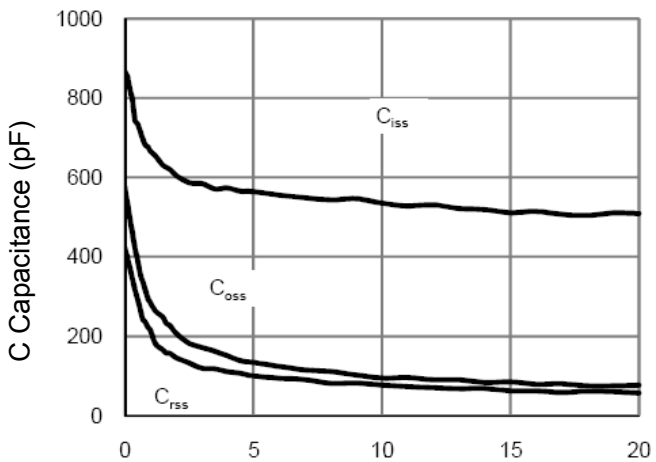
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 8 Power Dissipation**



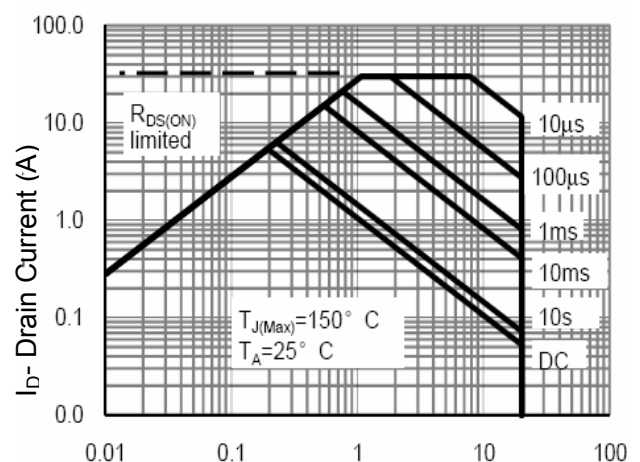
Qg Gate Charge (nC)  
**Figure 9 Gate Charge**



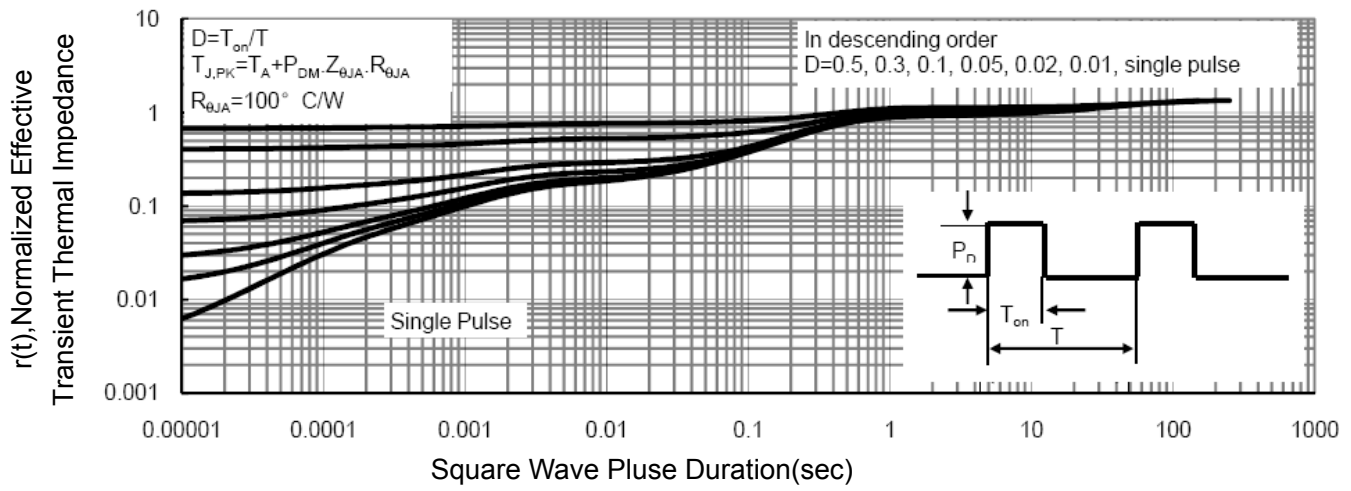
Vds Drain-Source Voltage (V)  
**Figure 10 Source- Drain Diode Forward**



Vds Drain-Source Voltage (V)  
**Figure 11 Capacitance vs Vds**



Vds Drain-Source Voltage (V)  
**Figure 12 Safe Operation Area**



**Figure 13 Normalized Maximum Transient Thermal Impedance**